CDF/DOC/CALORIMETRY/CDFR/3762
November 20, 1997
VERSION 1.0

Technical Design Report for the CDF Calorimeter and Shower Maximum Detector Front End Electronics Upgrade

A. Byon-Wagner[1], K. Byrum[2], G. Drake[1], G. W. Foster[1], S. Hahn[1], W. Hao[3], M. Lindgren[4], C. Nelson[1], L. Nodulman[2], V. Papadimitriou[3], T. Shaw[1], T. Zimmerman[1]

1) Fermi National Accelerator Laboratory
2) Argonne National Laboratory
3) Texas Tech University
4) University of California, Los Angeles

Abstract

The CDF experiment has engaged in an ambitious program to upgrade the calorimeter electronics to meet the challenge of operation after Main Injector commencement. The electronics described here are used primarily for photomultiplier tube readout, with the exception of those used for the central calorimeter strip and wire detector, which are gas based. This document describes the present plans for those electronics and their integration into the CDF environment.

1 Introduction

For the Tevatron RUN II the upgraded CDF detector must be capable of handling luminosity greater than $10^{32}\mathrm{cm}^{-2}\mathrm{sec}^{-1}$ and bunch spacing as small as 132 ns. The Plug Upgrade Calorimeter will replace the existing gas calorimeters. The new electromagnetic calorimeter is made of lead and scintillator tiles. The signal is read out by photomultiplier tubes(PMTs) located on the back plane of each endplug. The installation of new scintillator based calorimeters in the plug region allows a common design to be used for much of the front end electronics for the central and plug calorimeters and their associated preradiators and shower maximum detectors. The technology chosen for the digitization of the calorimeter signals is based on the charge integrating and encoding(QIE) chip [1] originally conceived for the SDC experiment and presently in production for use in KTeV experiment. It is intended to be used in conjunction with a ADC to digitize the PMT current pulses at a fast rate over a large dynamic range.

Section 2 gives the overview of the whole electronic readout system. The electronics for the central and plug calorimeters is described in the section 3. Section 4 describes the simplified QIE version, which will be used for the shower maximum detectors, and an additional preamplifier system used for the shower-max detector in the central region. In section 5 the system installation is discussed.

2 System overview

An overview of the digital data path of the calorimeter readout is shown in figure 1. The calorimeter analog information is received by the ADc/MEMory (ADMEM) modules, resided in 9U VME crates which replace the existing RABBIT crates in the collision hall.

The readout of the calorimeters is done by integrating the charge coming from the individual calorimeter photomultiplier tubes (figure 2). The function of the ADMEM modules will be to receive the analog signals, digitize them at a rate of up to 7.6 MHz, store them in a Level 1 pipeline buffer. The information from every calorimeter tower is summed and sent to the Level 1 trigger system. On receiving an Accept from the Level 1 trigger (after 42 beam crossing), the date are stored in one of four buffers until a Level 2

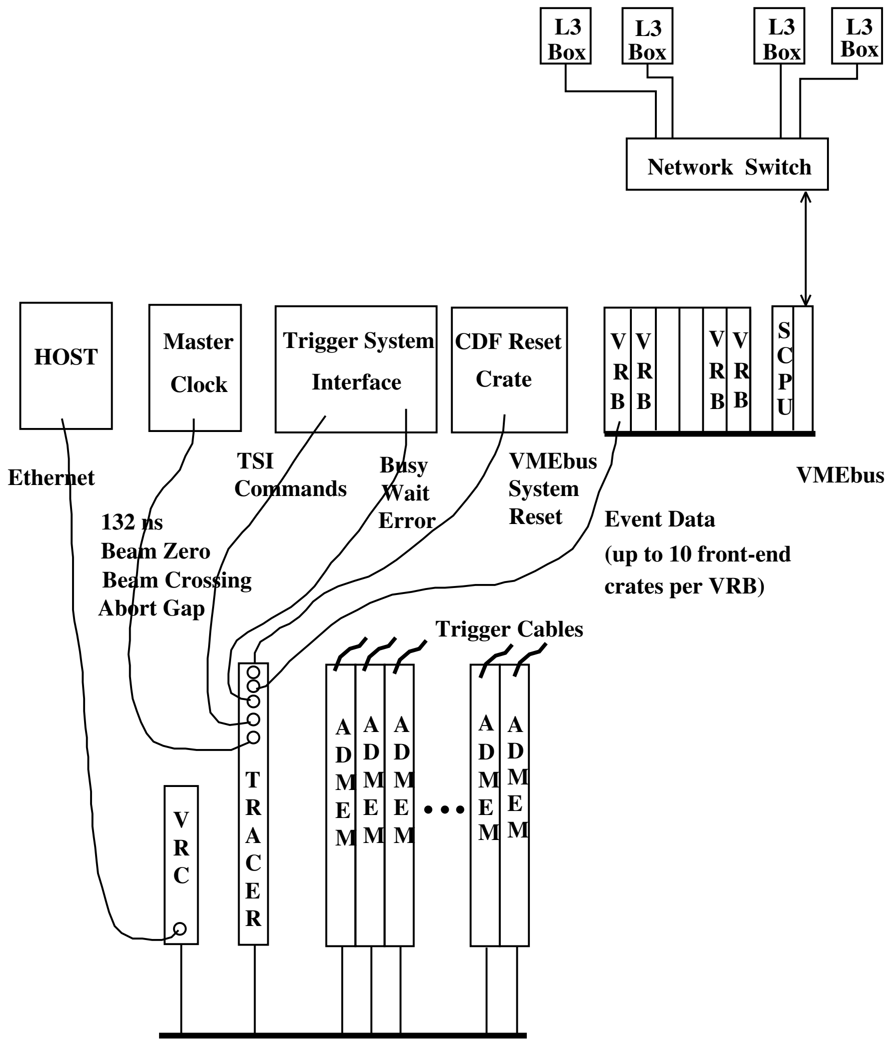

Figure 1: Digital Data Path Overview.

trigger decision is made. The data in the L2 Accept buffers will be readout via a VMEbus Readout Controller(VRC) and sent upstream on serial lines to VMEbus Readout Buffer(VRB) modules, from which it goes into the Level 3 processing farm.

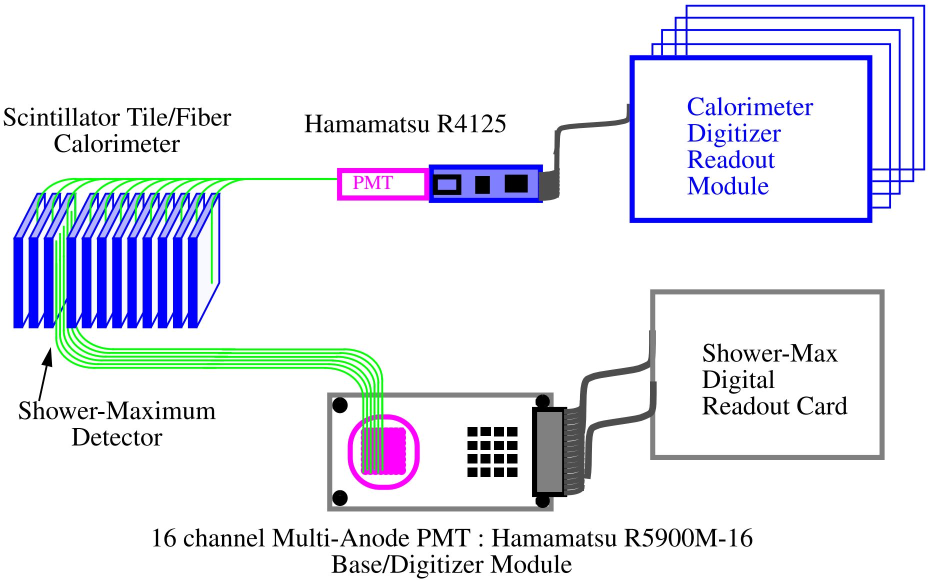

Figure 2: Calorimeter readout.

The communication with the Trigger System Interface (TSI) will be handled by the TRigger And Clock + Event Readout module (TRACER) located in the slot 2 of the VMEbus crate. The TRACER will receive signal from the Trigger supervisor, digitally process them and then fan them out to the ADMEM modules[4]. It also provided the path for sending the event data to higher level DAQ modules.

3 Calorimeter Electronics

3.1 Performance requirements

The dynamic range of the readout is set by physics requirements on the calorimeters, and by the PMT and scintillator characteristics. The estimation of the maximum signals that will be seen for the collider energy of 2 TeV and an integrated luminosity of 2 fb^{-1} has been made for all the calorimeters[2] using the RUN I data. The maximum energy deposited in the electromagnetic calorimeter tower will be 655GeV for the central and 750GeV for the plug, which is a factor of two larger than the data of Run I. In order to measure a signal as low as 1/10 of MIP energy (300MeV), 14 bits dynamic range is required. With the 2 bits for the pedestal separation and 1 bit for PMT channel to channel gain variations, more than 17 bits dynamic range is needed.

For the resolution requirement, study has been done on the W mass resolution due to the QIE digitization, using the $W \rightarrow e\nu$ event from Run 1a [1]. It is found that with the 8 or more bits ADC the error caused by the digitization is about 2-4 MeV, which is much smaller than expected accuracy on the W mass measurement (δM_W(Run II)$\leq$ 50 MeV).

The signals from the PMT's are about 80 nsec long. There is not enough time to integrate , read out and reset the integrating capacitors before the next bunch crossing, therefore the digitization must be pipelined. The summed digitized data is used to generate the Level-1 trigger as is used for the offline data analysis. The time needed to make a Level-1 decision is about 42 beam crossings($\sim 5.5\mu sec$), which requires the readout system to be fully pipelined with 42-event buffer for level-1 trigger and 4 additional buffers for Level-2 system.

The design of the ASIC has being modified to the CDF specifications (Appendix A). The full scale input charge of 1300 pC by increasing the integration capacitor to 2.5pF. It gives 5fC for the least count in I/2 range, which corresponding to 2.5 MeV.

3.2 ADMEM Boards

The readout module is mounted on an ADc/MEMory(ADMEM) VME board[3]. The analog Front-end portion of the ADMEM board will be implemented on removable Paddle boards(SMT board), which is 9 inch long and 4 inch wide. A single SMT board will be used to instrument each analog channel being fed into the ADMEM. Each ADMEM board will hold 20 of these front end modules.

[1] Based on Kim's presentation.

3.2.1 SMT board

A schematic of the front end module is shown in figure 3. It includes a current buffer, a charge injection circuit for calibration, a radioactive source current calibration circuit, the QIE, A 10 bit ADC to digitize the voltage presented by the QIE, and digital memory for converting the floating point QIE+ADC output to a dual range linear 16 bit number.

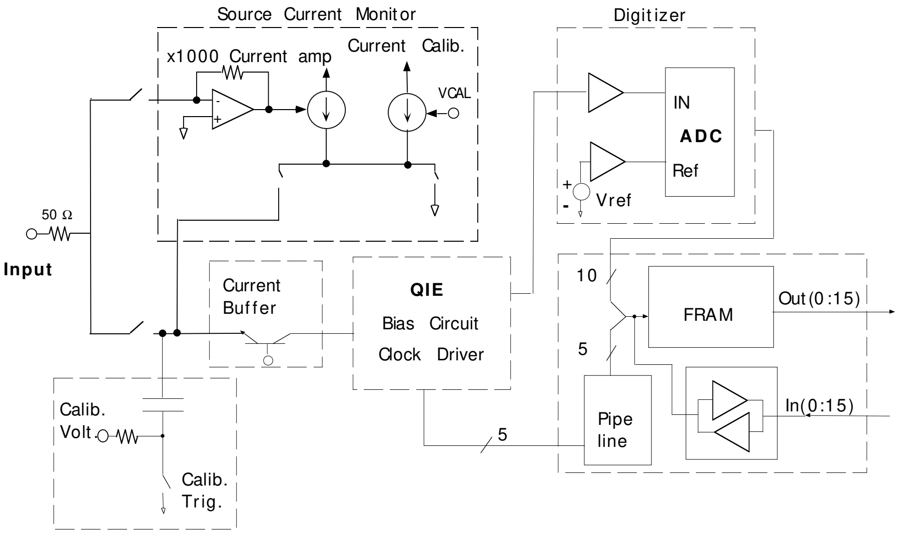

Figure 3: Simplified schematic of the front end module SMT.

QIE Operation:

Charge Integrating and Encoding(QIE) is the heart of the read module (figure 4). It has five major sections: A current splitter, a gated integrator/switch, a comparator, an encoder, and an analog multiplexer. The processing of signals within the chip is done in a four stage pipeline. In the first step, the current from PMT is split into 8 binary weighted current outputs. The outputs are supplied through 8 identical 2.6 pf integrating capacitors for one clock period. The voltage which is integrated on the capacitors is the largest on the I/2 range and decreases for each capacitor down to I/512 range. In the second step, the current switches to the next set of eight integrating capacitors. The capacitor voltage are applied to a bank of comparators in the second clock period. Only one of the eight capacitor voltages will be in the appropriate range and will be sent to the ADC for digitization. The latched outputs are encoded to form a three bit number, which is sent to the output for use as the exponent of a floating point number, while the ADC value forms the 10 bit mantissa. In the third step the selected capacitor voltage is send to ADC to be digitized. In the last step the capacitors are reset and ready for another signal. Since each of these operations requires approximately one clock period and each of the integrator block performs one of the four functions during a given clock period, therefore the device has no signal deadtime.

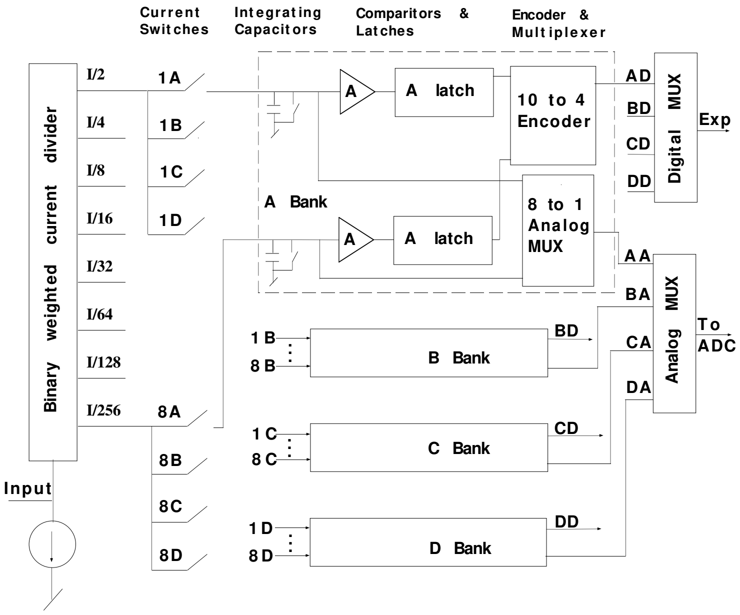

Figure 4: Simplified schematic of the QIE ASIC.

Current Buffer:

The input impedance of the QIE is not a constant 50Ω's, but varies as a function of the input current. This is not a problem when it is located close to the PMT base. In CDF the PMT's are mounted on the detectors and are connected to the readout crate via cables. To minimize the signal reflection, an external circuit (current buffer) has been designed for use between PMT base and QIE (figure 5). The photomultiplier signal current is pulled from the emitter of Q1 and is thus pulled from the output (the QIE) by Q1's collector. The input impedance is low (a few ohms), due to the standing current in Q1 pulled by the current source I2, and due to the action of the inverting amplifier formed by Q1 and Q2. The collector output impedance is high in comparison to the QIE input impedance, so the dynamic variations of the QIE impedance are unimportant. The current sources I1 must supply the same current pulled by I2 to avoid pulling I2's current from the QIE. The details which allow I1 and I2 to be closely matched are not shown. The current sources I3 is matched by I1 and I2 so that the base current from Q1 is approximately cancelled by Q2.

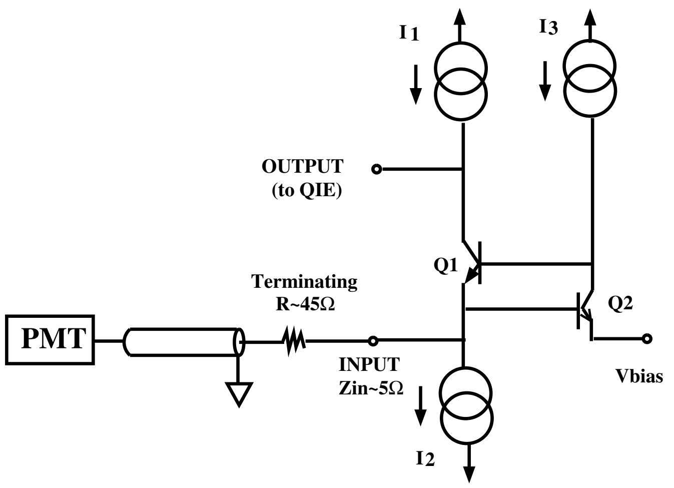

Figure 5: Simplified Schematic of Current Buffer.

The performance of prototype circuits in conjunction with the QIE has been excellent, maintaining the required linearity, with low power consumption ($\sim$ 50 mW).

Calibration:

A QIE has 32 integrating capacitors, 8 in each of the 4 pipelines. Several circuits have been designed and tested for possible use in injecting a known charge into the QIE to calibrate these capacitors. For each capacitor we plan to calibrate 5 points with different input charges. For each point 10 events are needed and the charge pulser recharge time is $100\mu s$. Therefore the total time will be 4capacitors$\times$8ranges$\times$5points$\times$10events$\times$$100\mu s$=.2seconds. The gains and offsets will be calculated from a least square linear fit.

The other calibration circuitry is needed to measure the DC current from the PMTs when a radioactive source is passed in front of the calorimeter scintillator. Both the plug and central calorimeter adjust PMT gains based on this calibration. The sources strength is such that the typical current from a PMT is about 100 nA, which integrates only 13 fC of charge in 132 ns. Half of the charge goes through the I/2 range. A 10 bit ADC gives 5.2 fC per count in the I/2 range. Therefore a circuit of high-gain (few hundred times) current amplifier is design to achieve the required measurement accuracy.

For the prototype SMT card, it is planned to put both the charge pulser and the current sources calibrator on the card. If we can put both on the card, then we can find out during the beam test or vertical slice tests, whether the charge pulser can be eliminated. It would be a reduction in cost and complexity, but not a huge reduction.

The output of the QIE will consist of 2 bit integrating capacitor ID, a 3 bit range ID and 10 bit ADC output, which gives 10 bits resolution. The total 16 bit information per event will be turned into a linearized 15 bit number, with a 1 bit range, in a 1 Mbyte Flash RAM. The Flash RAM is used as a look-up table that take out any range and capacitor information. It is reloaded with the conversion constants (gains and offsets) from the calibration procedure described above.

The power consumption has been estimated (Table 1), it is about 1.5 Watts per channel.

To the present, the test have been done using a version of ASIC that was the final preproduction version of the KTEV chip, along with an 8 bit FADC. The basis of the circuit at present is capacitive discharge using a precision voltage source. Initial tests were capable of measuring the middle ranges to the required accuracy. Figure 6 shows the digitization error as

Section	POWER (mW)
Current buffer	50
QIE and bias	650
digitizer	533
charge injector	5
digital section	285
source current monitor	15
Total	1538

Table 1: Estimated power consumption of front-end module.

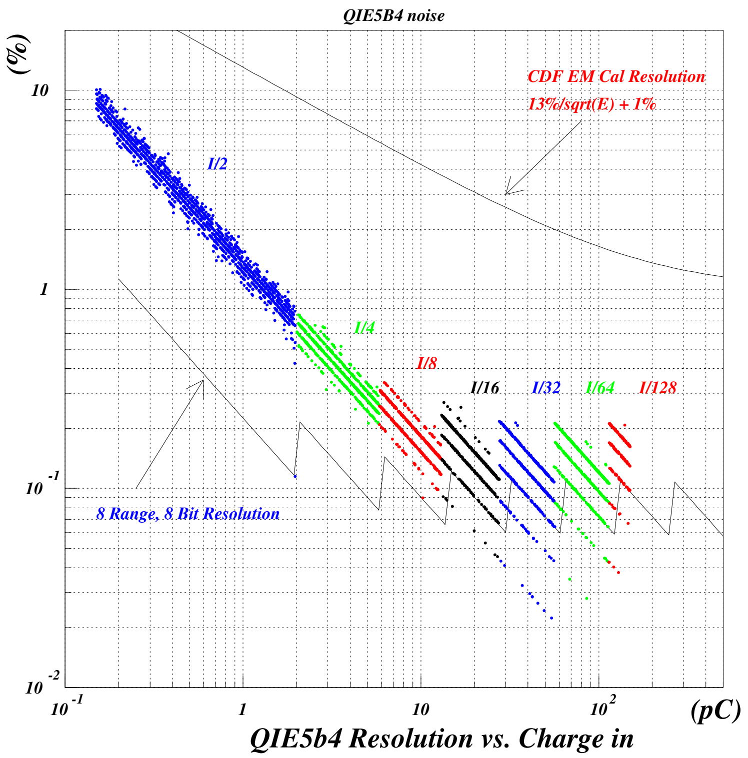

Figure 6: Digital resolution and Noise performance of prototype QIE5b4 ASIC as a function of input signal level.

a function of input charge. The bottom curve gives the digitization sigma (=least count/$\sqrt{12}$) for the floating-point output of the digitizer. The point is the result of the test using the KTeV chip. It also show the calorimeter energy resolution of $13\%/\sqrt{E}$ with a 1% constant term. Three types of 10-Bit ADC are considered for use. They are HI5710, ADS820 and AD876. The final decision will be made after the evaluation.

The first design of the CDF QIE6 was submitted for fabrication at the end of April. The new QIE6 prototype chip was received in July. The tests and measurements are in progress.

3.2.2 Digital Circuitry

The ADCs digitize the analog detector signal every beam crossing (132 ns). Digitized data is used for L1 trigger sums, transmitted upstairs on cables. The digitized data must also be stored in a digital pipeline for a period of 42 bunch crossings or 5.5μs. That is the period of time required for the level 1 trigger decision to reach the front-end crate. A level 1 Accept causes the data to be written into one of the four level 2 buffers, and a level 1 Reject causes the data to be discarded at the end of the storage pipeline. A level 2 accept cause the VMEbus Readout Controller (VRC) to address each ADMEM card within the create and do a block read of the channel data.

The digital pipeline and Level 2 buffer is implemented with Xilinx FPGAs, which is also mounted on the ADMEM board[3]. The device will take four channels digital data, form the trigger sums and pass that data to another FRAM which Et weights it and delivers a 10 bit number to the level 1 trigger. A separate diagnostic path allows the user to send a pre-determined set of diagnostic data through the pipeline chip.

3.2.3 Timing

The signal timing of the front-end modules is shown in figure 7. From the beam collision the signals will take 90ns to reach the front-end electronics, which includes 20ns of time-of-flight, 60ns of PMT propagation time and 20ns propagation in cable. QIE and ADC need $5 \times 132ns$ to integrate and digitize the signals. With the 2 clock cycles in Xilinx and one clock cycle in each of the FRAMs, it will take about 10 clock cycles to have the signal reach the trigger output.

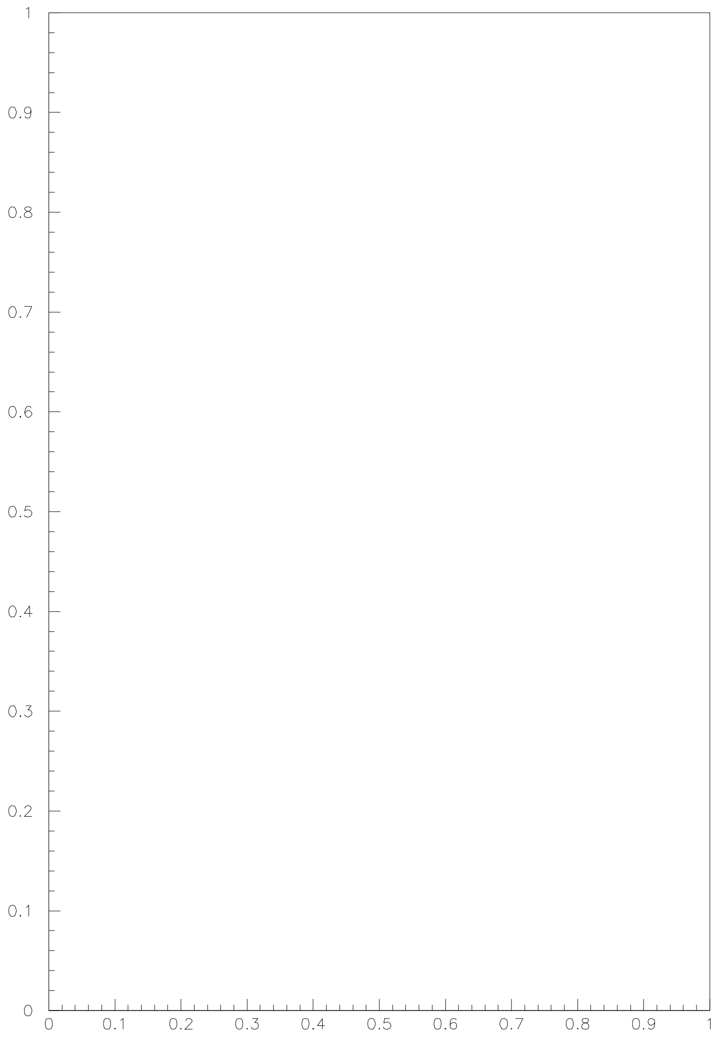

Figure 7: Front End Module Signal Timing

4 Shower Maximum Detector Electronics

The shower maximum and preshower detectors will also use the QIE technology. The main differences in the shower-max version are the reduced dynamic range and accuracy, which allow a low power consumption and cost per channel. The system has two components, digitizer card and readout board(figure 8). the photodetector for plug shower-max calorimeter is16 channel Multi-Anode PM Tube(Hamamatsu R5900M-16). The digitizer module includes QIE, ADC, Level-1 and Level-2 storages. The digitizer cards are mounted close to the detector, instead of on a VME board with the digital readout card.

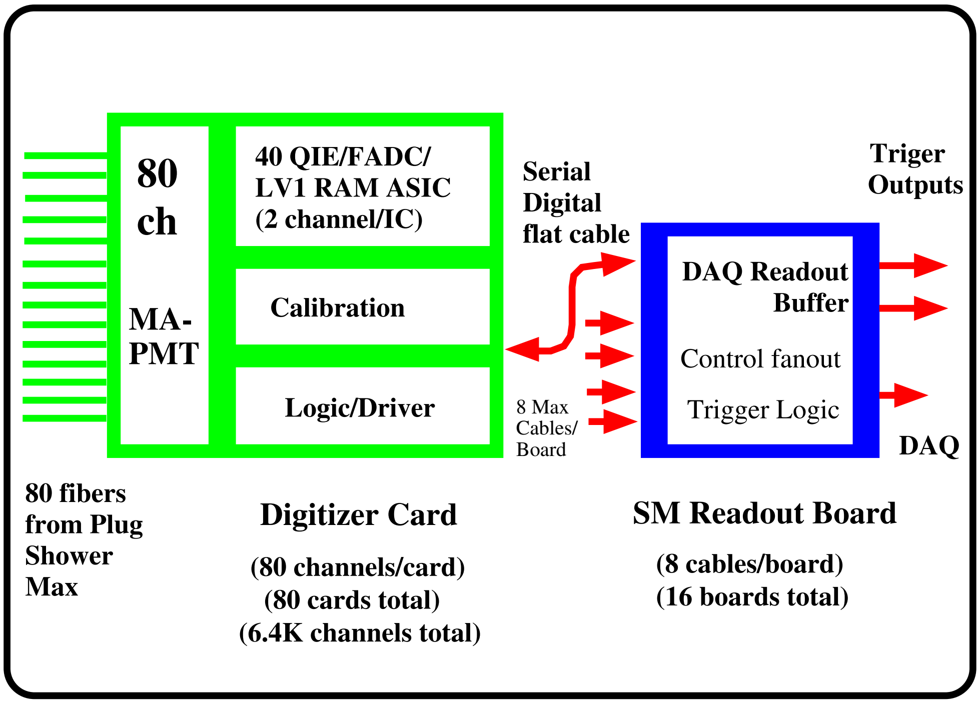

Figure 8: Schematic showing the general layout of the shower-max digitizer boards.

4.1 Shower-Max Performance requirements

The requirements for the plug shower-max detector electronics are outlined in the reference [5]. The required dynamic range is 12-14 bits. 8 bits device (5-bit mantissa and 3-bit exponent) gives the maximum error $\pm 1.5\%$, which will not degrade the position resolution of the shower-max detectors. The linearity should be better than 3%, since the Shower-max detector itself is grossly nonlinear due to shower depth change with energy. The cross talk should be less than 2%.

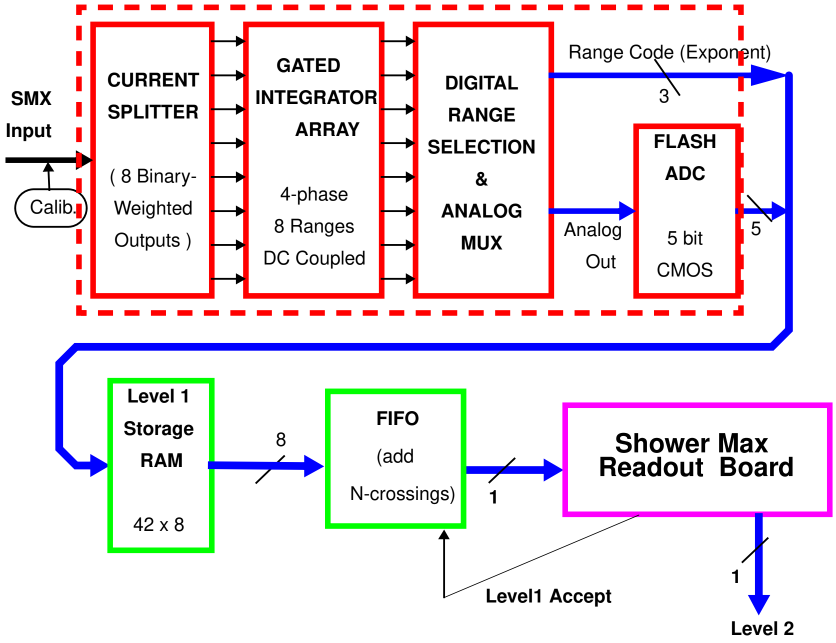

Figure 9: Shower-max digitizer block diagram.

4.2 Shower-Max Digitizer cards

The Shower-Max QIE, SMQIE, will be a different chip than calorimeter QIE. It is a single-ended splitter rather than the differential splitter in the normal QIE. The basic circuit is a multi-transistor active cascade stage, with the "collectors" of the series-pass transistors grouped together in binary segments to split the current output according to how many transistors are in each group. The input rests at +0.8V (one gate threshold) above ground when the chip is running from a +5V supply. The digitizer also contains a gated integrator array which integrated the charge from each scale on one of the four capacitors in a pipelined manner, digital range selection, 5 bits flash ADC and Level 1 storage RAM (figure 9). With the sufficient integrating capacitance matching, channel by channel calibrating constants will not be needed. The summary of the overall basic design is listed in Appendix B.

Each digitizer card contains 80 (32 for the central shower-max detector) channels which are connected to a VME shower-max readout board via flat cables.

4.3 Central Shower-Max Preamplifier

The central calorimeter shower-max proportional chambers measure the charge deposition on orthogonal strip and wires. In the run-I configuration, the rabbit electronics matched the gain of the strip and wire signals, giving the same dynamic range to both. In the upgrade run-II configuration, we plan to use a preamplifier circuit to match the gains in both views. As described in the previous section, separately-housed front-end cards will contain both the preamplifier circuit and the shower-max QIE. The digitized output from these cards will be multiplexed and sent to the DAQ electronics and to the trigger as shown in figure 10. The front-end card will be mounted at the rear of the detector wedge as close as possible to where the cables emerge.

One of the key criteria for the selection of a preamplifier is the intrinsic noise of the circuit. Since the strip signal is sensitive to digital traffic, we want our preamplifier circuit to introduce minimal additional noise. Noise sensitivity has always been a problem in the CES in the past, in spite of the careful separation in time of the digital activity at the front-end electronics from the sensitive analog signal acquisition and processing. In run-II we expect the noise to be worse since the digital activity will occur during analog signal processing. Recent noise measurements performed on the CES chamber at B0 showed that digital noise could be reduced by a factor of 2-5 by using a different detector scheme. This additional reduction could impact where we mount the housed front-end cards, giving us more flexibility.

Specifications for the preamplifier include that the power consumption be less than 1kWatt per chamber wedge, the QIE must see a constant current and the output preamplifier current never be positive, the bandwidth of operation be 7-50MHz, and the signal supply be +5Volts. In addition, another feature of the central strip and wire signals is the long signal rise time (τ_{rise}=530ns and τ_{strip}=640ns), therefore the integration over 3-4 crossings is needed. We plan to digitize the signals at every 132 ns, but add 3-4 consecutive time slice windows..

4.4 Shower-Max Readout board

The general layout of the shower-max VME readout boards is shown in figure 10. They are located in crate mounted on the detector. This card simply receives the serial digitized data from each digitizer module and store it for DAQ readout over the crate backplane. It also fans out clock, power and trigger/control signals to the digitizer modules.

5 System Installation

Figure 11 shows the position of racks for one arch of the central calorimeter. According to the current plan, each rack serves6 wedges and contains three VME crates, power supplies, a fan and two heat exchangers between VME crates for the chilled water cooling. The advantage of having crates in a rotatable rack is that they are easy to access and the water leaks are more easily contained. One disadvantage is that the signal may have to go through long cables to reach the crates. Because of space constraints, it is not known yet if the racks will be hinged in the inner side or outer side of the detector. Because of this decision, the cable may be shorter or longer.

Figure 12 shows two possible schemes of mounting the VME crates around the plug detector. Again we will mount the crate either individually or in rotatable racks. In this case one has to take into account an additional space constraints due to the muon arches. The Shower-Max QIE digitizer boxes are mounted at the top of PMT boxes and the PMT boxes have air cooling using fans.

The grounding of the calorimeters will be done according to the scheme discussed in the reference[6].

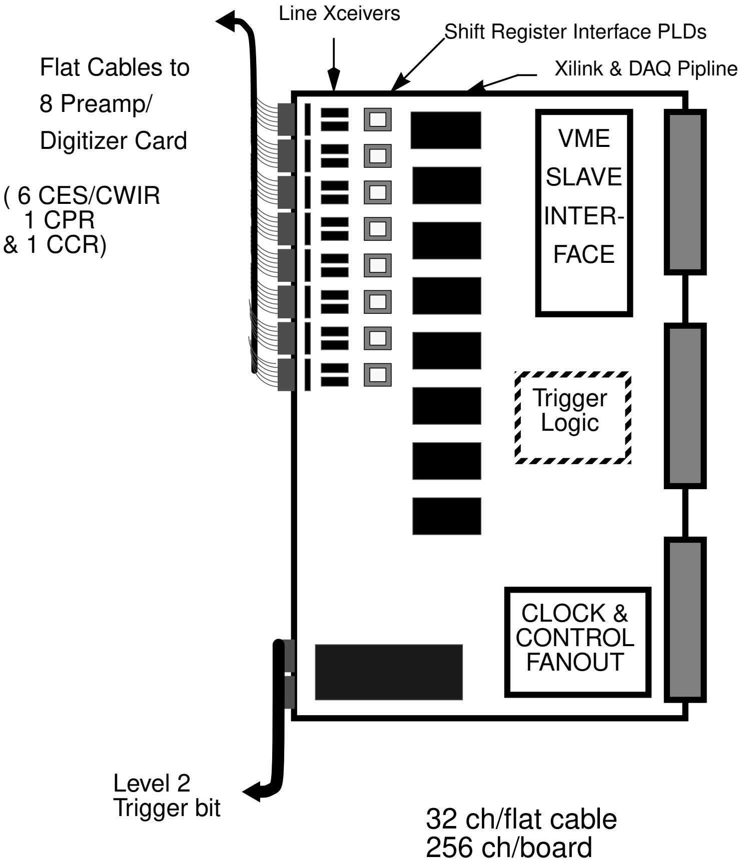

Figure 10: Schematic showing the general layout of the shower-max VME readout boards.

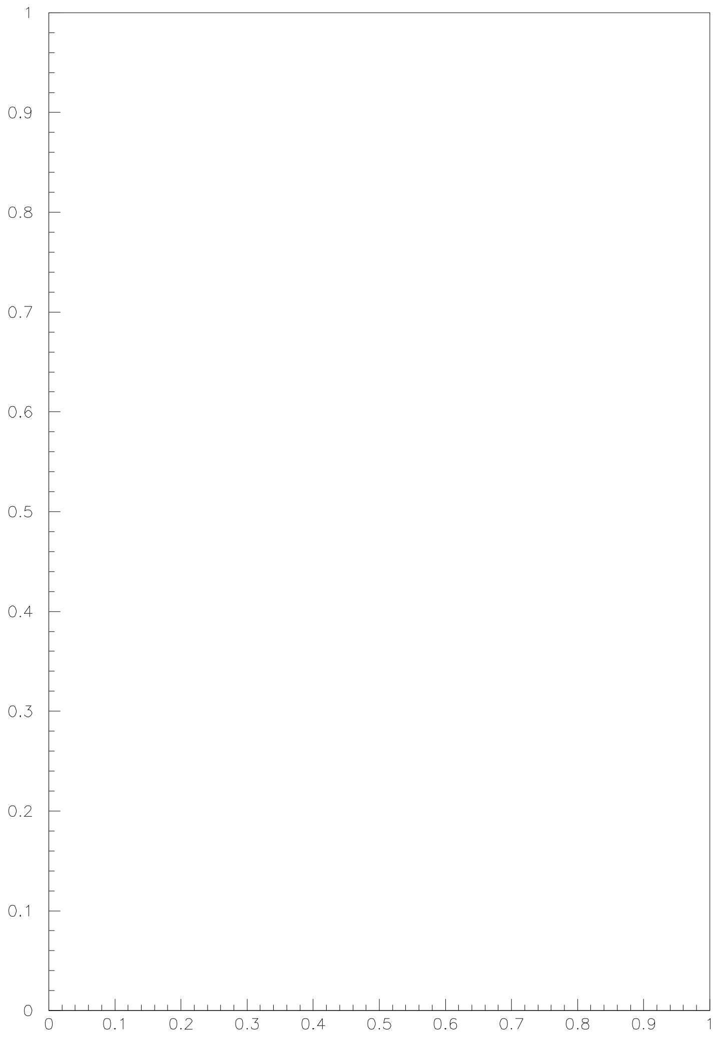

Figure 11: Layout of VME crate for central calorimeter

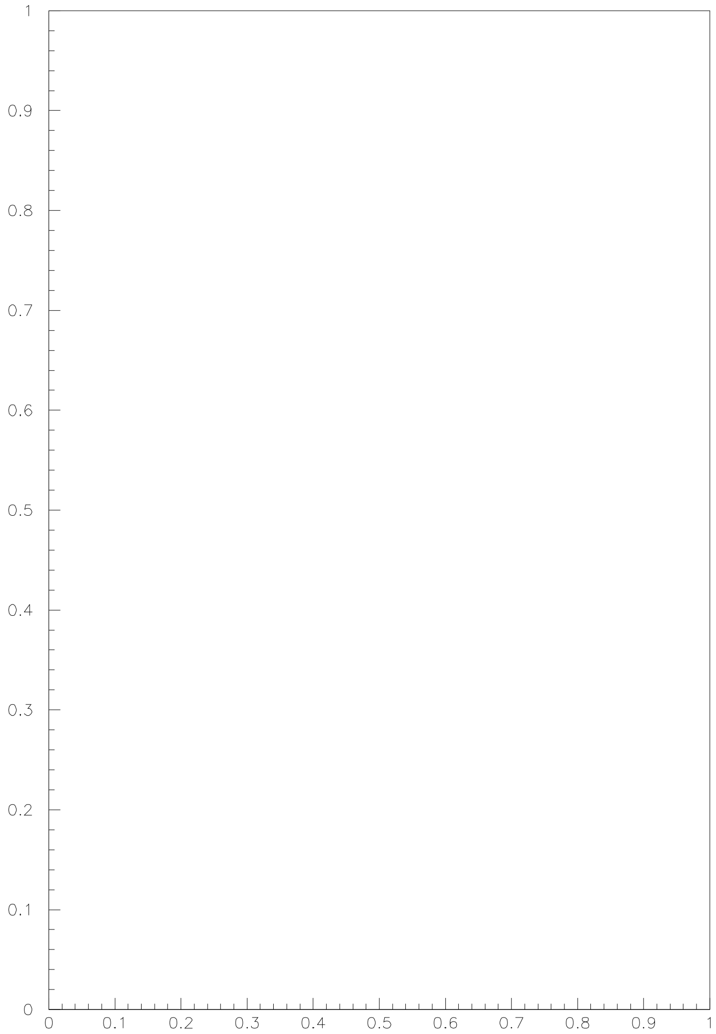

Figure 12: Layout of VME crate, QIE box and PMT box for plug calorimeter

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[6] G. Drake and C. Nelson, "Grounding the CDF Detector", Presentation at CDF Frontend/Trigger/DAQ Workshop in Ann Arbor, 21-23 August 1996.

Appendix A. Specifications for CDF QIE

1. Analog Input	
Full scale input charge	-1300pC
Max. instantaneous current	-50mA
Quiescent voltage	+1 volt, nominal
Small signal impedance	150 ohms, or less
Maximum voltage swing	-2.7 volts, from quiescent level
2. Analog Output	
Mode	Differential
Differential output range	0 to 1 volt, nominal
Common mode	Between +3 and +9 volts is acceptable
output settling	Driving a 10 pF load, the output must settle sufficiently within 100 nsec after the corresponding clock edge that the other specifications are met, particularly linearity and stability.
Output Drop rate	Less than 1 mv per nsec, after 100 nsec of settling time.
Equivalent noise charge	Less than 0.2% of input charge or 10fc, whichever is greater.
3. Digital I/O	
Input	Clock and Reset
Input Levels	Single-ended TTL, internally buffered
Clock frequency	7.6MHz (1/132nsec)
RESET operation	to be completed within 50ns after assertion
Outputs	3 Current range bits and 2 capacitor ID bits
Output Levels	Single-ended TTL
Output settling	With a 10 pF load, the data must be valid within 50ns after corresponding clock edge.

4. Linearity and Stability	
Linearity	The linearity of each of the 32 response ranges must be such that a straight line fit of any range will allow the input charge to be reconstructed to within 0.2% of itself or 10fC, whichever is greater.
Temperature stability	The reconstructed input charge must vary by less than $0.2\%/^\circ C$, or $10\text{fC}/^\circ C$, whichever is greater.
Time stability	The reconstructed input charge must vary by less than the greater of either 0.2% or 10fC in any four hour period.
Power supply dependance	The reconstructed input charge must vary by less than 0.2% or 10fC, whichever is greater, for a 1% or 50mV change in any supply voltage.
5. Power supply	
Voltage	Positive supply voltage and ground. Exact value to be determined by the IC designer
6. Operating Environment	
Temperature range	20 degree C. to 55 degree C.

Appendix B. Summary of the SMQIE basic design

- Scaled-down version of calorimeter QIE with FADC.
- Deadtimeless Charge Integration.
- Automatic Range Selection.
- 5 Bit Flash Digitization.
- 13-Bit Dynamic range.
- analog accuracy: error $\sim 3\%$ of signal size.
- 7-50 MHz operation.
- controlled input impedance (cable-compatible input).
- on-chip Level 1 Delay storage RAM (~ 44 storage locations).
- on chip Level 2 Buffer registers.
- daisy-chained serial readout.
- on-chip digital comparator for trigger output bit.
- on-chip calibration circuitry.
- on-chip PMT current measurement circuitry.
- 2 channel per tiny chip.
- single +5V supply.
- power $\leq$ 100mW/channel.